ADuC842 MicroConverter®, 12- Bit ADCs and DACs with Embedded Hi-Speed 62KB FLASH MCU

Preliminary Technical Data ADuC842

FEATURES

PIN COMPATABLE
- Upgrade to ADuC812/ADuC832

INCREASED PERFORMANCE
- Single Cycle 16MIPS 8052 core
- High Speed 400kSPS 12-Bit ADC

INCREASED MEMORY
- 62Kbytes On-Chip Flash/EE Program Memory
- 4KBytes On-Chip Flash/EE Data Memory
- In circuit re-programmable
- Flash/EE, 100 Yr Retention, 100 Kcycles Endurance
- 2304 Bytes On-Chip Data RAM

SMALLER PACKAGE
- Available in 8mm x 8mm Chip Scale Package
- Also available in 52 pin PQFP - pin compatable with ADuC812/ADuC831

ANALOG I/O
- 8-Channel, 400kSPS High Accuracy, 12-Bit ADC
- On-Chip, 20 ppm/°C Voltage Reference
- DMA Controller, High-Speed ADC-to-RAM capture
- Two 12-Bit Voltage Output DACs
- Dual Output PWM-ΣΔ DACs
- On-Chip Temperature Monitor Function

8051 Based Core
- 8051-Compatible Instruction Set (16.7 MHz Max)
- High performance Single Cycle Core*
- 32kHz Ext Crystal,On-Chip Programmable-PLL
- 12 Interrupt Sources, Two Priority Levels
- Dual Data Pointers, Extended 11-bit Stack Pointer

On-Chip Peripherals
- Time Interval Counter (TIC)
- UART, I2C and SPI® Serial I/O
- Watchdog Timer (WDT),
- Power Supply Monitor (PSM)

Power
- Normal: 6mA @ 5 V (Core CLK = 2.098 MHz)
- Power-Down: 15μA @ 3 V
- Development Tools
- Low Cost, comprehensive development system incorporating non-intrusive single pin emulation
- IDE based, assembly and C source debug

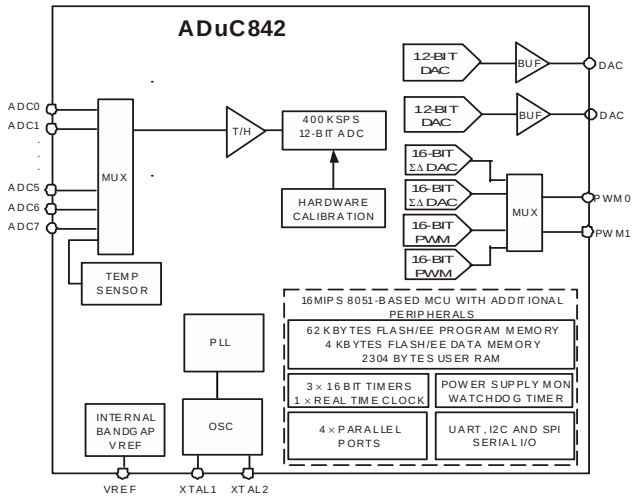
APPLICATIONS

Optical Networking - Laser Power Control
Basestation Systems
Precision Instrumentation, Smart Sensors
Transient Capture Systems
DAS and Communications Systems

MicroConverter is a registered trademark of Analog Devices, Inc.
SPI is a registered trademark of Motorola Inc.
* 68% of insturctions completed in one or two clock cycles

REV. PrB

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADuC842 is a complete smart transducer front-end, integrating a high-performance self calibrating multichannel ADC, dual DAC and an optimized single cycle 16MHz 8-bit MCU(8051 instruction set compatible) on a single chip.
The device operates from a 32 kHz crystal with an on-chip PLL generating a high-frequency clock of 16.77MHz. This clock is, in turn, routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller is an optimized 8052 core offering up to 16 MIPS peak performance. 62 Kbytes of nonvolatile Flash/EE program memory are provided on-chip. 4 Kbytes of nonvolatile Flash/EE data memory, 256 bytes RAM and 2 KBytes of extended RAM are also integrated on-chip.

The ADuC842 also incorporates additional analog functionality with two 12-bit DACs, power supply monitor, and a bandgap reference. On-chip digital peripherals include two 16-bit ΣΔ DACs, dual output 16-bit PWM, watchdog timer, time interval counter, three timers/counters, and three serial I/O ports (SPI, I2C and UART).

On the ADuC812 and ADuC832 the I2C and SPI interfaces shared some of the same pins. For backwards compatability this is also the case for the ADuC842. However, there is also the option to allow SPI operate separately on P3.3, P3.4 and P3.5 while I2C uses the standard pins. The I2C interface has also been enhanced to offer repeated start, general call and quad addressing.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the EA pin. A functional block diagram of the ADuC842 is shown above.

The part is specified for 3V and 5V operation with a maximum operating frequency of 16.777MHz.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

ADuC842–SPECIFICATIONS[1]

(AV_{DD} = DV_{DD} = 2.7V to 3.3V or 4.5V to 5.5V. V_{REF} = 2.5 V Internal Reference, Fcore = 16.777 MHz, All specifications T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS				
DC ACCURACY[2,3]				f_{SAMPLE} = 147 kHz,
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1	LSB max	2.5V Internal Reference
	±0.3	±0.3	LSB typ	
Differential Nonlinearity	±0.9	±0.9	LSB max	2.5V Internal Reference
	±0.25	±0.25	LSB typ	
Integral Nonlinearity[9]	±1.5	±1.5	LSB max	1V External Reference
Differential Nonlinearity[9]	+1.5/-0.9	+1.5/-0.9	LSB max	1V External Reference
Code Distrbution	1	1	LSB typ	ADC Input is a DC Voltage
CALIBRATED ENDPOINT ERRORS[4,5]				
Offset Error	±2	±3	LSB max	
Offset Error Match	±1	±1	LSB typ	
Gain Error	±2	±3	LSB max	
Gain Error Match	–85	–85	dB typ	
DYNAMIC PERFORMANCE				f_{IN} = 10 kHz Sine Wave f_{SAMPLE} = 147 kHz
Signal-to-Noise Ratio (SNR)[6]	71	71	dB typ	
Total Harmonic Distortion (THD)	–85	–85	dB typ	
Peak Harmonic or Spurious Noise	–85	–85	dB typ	
Channel-to-Channel Crosstalk[7]	–80	–80	dB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	
Leakage Current	±1	±1	µA max	
Input Capacitance	32	32	pF typ	
TEMPERATURE SENSOR[8]				
Voltage Output at 25°C	650	650	mV typ	
Voltage TC	–2.0	–2.0	mV/°C typ	
Accuracy	±3	±3	°C typ	Internal 2.5V V_{REF}
Accuracy	±1.5	±1.5	°C typ	External 2.5V V_{REF}
DAC CHANNEL SPECIFICATIONS				DAC Load to AGND
Internal Buffer Enabled				R_L = 10kΩ, C_L = 100 pF
DC ACCURACY[10]				
Resolution	12	12	Bits	
Relative Accuracy	±3	±3	LSB typ	
Differential Nonlinearity[11]	-1	-1	LSB max	Guaranteed 12-Bit Monotonic
		±1/2	±1/2	LSB typ
Offset Error	±50	±50	mV max	V_{REF} Range
Gain Error	±1	±1	% max	AV_{DD} Range
	±1	±1	% typ	VREF Range
Gain Error Mismatch	0.5	0.5	% typ	% of Full-Scale on DAC1
ANALOG OUTPUTS				
Voltage Range_0	0 to V_{REF}	0 to V_{REF}	V typ	DAC V_{REF} = 2.5V
Voltage Range_1	0 to V_{DD}	0 to V_{DD}	V typ	DAC V_{REF} = V_{DD}
Output Impedance	0.5	0.5	Ω typ	
I_{SINK}	50	50	µA typ	
DAC AC CHARACTERISTICS				
Voltage Output Settling Time	15	15	µs typ	Full-Scale Settling Time to Within 1/2 LSB of Final Value
Digital-to-Analog Glitch Energy	10	10	nV sec typ	1 LSB Change at Major Carry

Parameter	V_{DD} = 5 V	V_{DD} = 3 V	Unit	Test Conditions/Comments
DAC CHANNEL SPECIFICATIONS[12,13] Internal Buffer Disabled				
DC ACCURACY[10]				
Resolution	12	12	Bits	
Relative Accuracy	±3	±3	LSB typ	
Differential Nonlinearity[11]	-1	-1	LSB max	Guaranteed 12-Bit Monotonic
	±1/2	±1/2	LSB typ	
Offset Error	±10	±10	mV max	V_{REF} Range
Gain Error	±1	±1	% typ	VREF Range
Gain Error Mismatch	0.5	0.5	% typ	% of Full-Scale on DAC1
ANALOG OUTPUTS				
Voltage Range_0	0 to V_{REF}	0 to V_{REF}	V typ	DAC V_{REF} = 2.5V
REFERENCE INPUT/OUTPUT				
REFERENCE OUPUT[14]				
Output Voltage (V_{REF})	2.5	2.5	V	
Accuracy	±2.5	±2.5	% max	Of V_{REF} measured at the C_{REF} pin
Power Supply Rejection	47	57	dB typ	
Reference Temperature Coefficient	±20	±20	ppm/°C typ	
Internal V_{REF} Power-On Time	80	80	ms typ	
EXTERNAL REFERNCE INPUT[15]				
Voltage Range (V_{REF})[9]	0.1	0.1	V min	
	V_{DD}	V_{DD}	V max	
Input Impedance	20	20	kΩ typ	
Input Leakage	10	10	µA max	Internal Band Gap Deselected via ADCCON1.6
POWER SUPPLY MONITOR (PSM)				
DV_{DD} Trip Point Selection Range	2.63		Vmin	Four Trip Points Selectable in This Range Programmed via TPD1–0 in PSMCON
	4.37		Vmax	
DV_{DD} Power Supply Trip Point Accuracy	±3.5		% max	
WATCH DOG TIMER (WDT)[9]				
Time-out Period	0	0	ms min	Nine Time-out Periods
	2000	2000	ms max.	Selectable in This Range
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS[16]				
Endurance[17]	100,000	100,000	Cycles min	
Data Retention[18]	100	100	Years min	
DIGITAL INPUTS				
Input High Voltage (V_{INH})	2.4		V min	
Input Low Voltage (V_{INL})	0.8		V max	
Input Leakage Current (Port 0,1, EA)	±10		µA max	V_{IN} = 0 V or V_{DD}
	±1	±1	µA typ	V_{IN} = 0 V or V_{DD}
Logic 1 Input Current				
(All Digital Inputs)	±10		µA max	V_{IN} = V_{DD}
	±1	±1	µA typ	V_{IN} = V_{DD}
Logic 0 Input Current (Port 2, 3)	–80		µA max	
	–40	–40	µA typ	V_{IL} = 0 V
Logic 1-0 Transition Current (Port 2, 3)	–700		µA max	V_{IL} = 2 V
	–400	–400	µA typ	V_{IL} = 2 V
CRYSTAL OSCILLATOR				
Logic Inputs, XTAL1 Only				
VINL, Input Low Voltage	0.8	0.4	V typ	
VINH, Input High Voltage	3.5	2.5	V typ	

ADuC842–SPECIFICATIONS[1]

Parameter	V_{DD}=5V	V_{DD}=3V	Units	Test Conditions
XTAL1 Input Capacitance	18	18	pF typ	
XTAL2 Output Capacitance	18	18	pF typ	
MCU Clock Rate	16.777216	16.777216	MHz max	
DIGITAL OUTPUTS				
Output High Voltage (V_{OH})	2.4	2.4	V min	V_{DD} = 4.5 V to 5.5 V I_{SOURCE} = 80 µA
	4.0	2.6	V typ	V_{DD} = 2.7 V to 3.3 V I_{SOURCE} = 20 µA
Output Low Voltage (V_{OL})				
ALE, Ports 0 and 2	0.4	0.4	V max	I_{SINK} = 1.6 mA
	0.2	0.2	V typ	I_{SINK} = 1.6 mA
Port 3	0.4	0.4	Vmax	I_{SINK} = 4 mA
SCLOCK/SDATA	0.4	0.4	Vmax	I_{SINK} = 8 mA
Floating State Leakage Current	±10	±10	µA max	
	±1	±1	µA typ	
Floating State Output Capacitance	10	10	pF typ	
START UP TIME				Core CLK = 16MHz
At Power-On	500	500	ms typ	
From Idle Mode	100	100	µs typ	
From Power-Down Mode				
Wakeup with INT0 Interrupt	150	400	ms typ	
Wakeup with SPI/I^2C Interrupt	150	400	ms typ	
Wakeup with External RESET	150	400	ms typ	
After External RESET in Normal Mode	3	3	ms typ	
After WDT Reset in Normal Mode	3	3	ms typ	Controlled via WDCON SFR
POWER REQUIREMENTS [19,20]				
Power Supply Voltages				
AV_{DD} / DV_{DD} - AGND		2.7	V min.	AV_{DD} / DV_{DD} = 3V nom.
		3.3	V max.	
	4.5		V min.	AV_{DD} / DV_{DD} = 5V nom.
	5.5		V max.	
Power Supply Currents Normal Mode				
D_{VDD} Current[9]	12	6	mA typ	Fcore = 8 MHz (CD=3)
A_{VDD} Current[9]	1.4	1.4	mA max	
D_{VDD} Current	25	n/a	mA max	Fcore = 16 MHz (CD=0)
	21	n/a	mA typ	
A_{VDD} Current	1.4	n/a	mA max	
Power Supply Currents Idle Mode				
D_{VDD} Current[9]	5	2.5	mA typ	Fcore = 8 MHz (CD=3)
A_{VDD} Current[9]	0.11	0.11	mA typ	
D_{VDD} Current[9]	11	n/a	mA max	Fcore =16 MHz (CD=0)
	10	n/a	mA typ	
A_{VDD} Current[9]	0.11	n/a	mA typ	
Power Supply Currents Power Down Mode				For any Core CLK
A_{VDD} Current	3	2.5	uA typ	
D_{VDD} Current	35	15	uA max	osc off
	25	12	uA typ	
	120	120	uA typ	osc on
Typical Additional Power Supply Currents				AVDD = DVDD = 5V
PSM Peripheral	50		uA typ	
ADC	1.5		mA typ	
DAC	150		uA typ	

NOTES

[1] Temperature Range -40ºC to +85ºC.

[2] ADC Linearity is guaranteed during normal MicroConverter Core operation.

[3] ADC LSB Size = Vref / 2^12 i.e for Internal Vref=2.5V, 1LSB = 610uV and for External Vref =1V, 1LSB = 244uV.

[4] Offset and Gain Error and Offset and Gain Error Match are measured after factory calibration.

[5] Based on external ADC system components the user may need to execute a system calibration to remove additional external channel errors and achieve these specifications.

[6] SNR calculation includes distortion and noise components.

[7] Channel to Channel Crosstalk is measured on adjacent channels.

[8] The Temperature Monitor will give a measure of the die temperature directly, air temperature can be inferred from this result.

[9] These numbers are not production tested but are guaranteed by Design and/or Characterization data on production release.

[10] DAC linearity is calculated using :
reduced code range of 48 to 4095, 0 to Vref range.
reduced code range of 48 to 3945, 0 to V_{DD} range.
DAC Output Load = 10K Ohms and 100 pF.

[11] DAC Differential NonLinearity specified on 0 to Vref and 0 to Vdd ranges

[12] DAC specification for output impedance in the unbuffered case depends on DAC code

[13] DAC specifications for Isink, voltage output settling time and digital-to-analog glitch engergy depend on external buffer implementation in unbuffered mode.

[14] Measured with Vref and Cref pins decoupled with 0.1µF capacitors to graound. Power-up time for the Internal Reference will be determined by the value of the decoupling capacitor chosen for both the Vref and Cref pins.

[15] When using an External Reference device, the internal bandgap reference input can be bypassed by setting the ADCCON1.6 bit. In this mode the Vref and Cref pins need to be shorted together for correct operation.

[16] Flash/EE Memory Reliability Characteristics apply to both the Flash/EE program memory and the Flash/EE data memory.

[17] Endurance is qualified to 100 Kcycles as per JEDEC Std. 22 method A117 and measured at -40ºC, +25ºC, and +85ºC, typical endurance at 25ºC is 700 Kcycles.

[18] Retention lifetime equivalent at junction temperature (Tj) = 55ºC as per JEDEC Std. 22 method A117. Retention lifetime based on an activation energy of 0.6eV will derate with junction temperature as shown in Figure 27 in the Flash/EE Memory description section of this data sheet.

[19] Power Supply current consumption is measured in Normal, Idle, and Power-Down Modes under the following conditions:

Normal Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, Core Executing internal software loop.

Idle Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, PCON.0=1, Core Execution suspended in idle mode.

Power-Down Mode: Reset = 0.4 V, All Port 0 pins = 0.4 V, All other digital I/O and Port 1 pins are open circuit, Core Clk changed via CD bits in PLLCON, PCON.0=1, Core Execution suspended inpower-down mode, OSC turned ON or OFF via OSC_PD bit (PLLCON.7) in PLLCON SFR

[20] D_{VDD} power supply current will increase typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

Specifications subject to change without notice.

ADuC842

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

AV_{DD} to DV_{DD} ..... –0.3 V to +0.3 V
AGND to DGND ..... –0.3 V to +0.3 V
DV_{DD} to DGND, AV_{DD} to AGND .... –0.3 V to +7 V
Digital Input Voltage to DGND –0.3 V, DV_{DD} + 0.3 V
Digital Output Voltage to DGND –0.3 V, DV_{DD} + 0.3 V
V_{REF} to AGND ..... –0.3 V, AV_{DD} + 0.3 V
Analog Inputs to AGND ..... –0.3 V, AV_{DD} + 0.3 V
Operating Temperature Range Industrial ADuC842BS
..... –40°C to +85°C
Operating Temperature Range Industrial ADuC842BCP
..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
θ_{JA} Thermal Impedance (ADuC831BS) ..... 90°C/W
θ_{JA} Thermal Impedance (ADuC831BCP) ..... 52°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADuC842BS	–40°C to +85°C	52-Lead Plastic Quad Flatpack	S-52
ADuC842BCP	–40°C to +85°C	56-Lead Chip Scale Package	CP-56

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADuC842 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Mnemonic	Type	Function
DV_{DD}	P	Digital Positive Supply Voltage, 3 V or 5 V Nominal
AV_{DD}	P	Analog Positive Supply Voltage, 3 V or 5 V Nominal
C_{REF}	I	Decoupling Input for On-Chip Reference. Connect 0.1 µF between this pin and AGND.
V_{REF}	I/O	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the reference source for the analog-to-digital converter. The nominal internal reference voltage is 2.5 V and this appears at the pin. This pin can be overdriven by an external reference.
AGND	G	Analog Ground. Ground Reference point for the analog circuitry.
P1.0–P1.7	I	Port 1 is an 8-bit Input Port only. Unlike other Ports, Port 1 defaults to Analog Input Mode, to configure any of these Port Pins as a digital input, write a "0" to the port bit. Port 1 pins are multifunction and share the following functionality.
ADC0–ADC7	I	Analog Inputs. Eight single-ended analog inputs. Channel selection is via ADCCON2 SFR.
T2	I	Timer 2 Digital Input. Input to Timer/Counter 2. When Enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
T2EX	I	Digital Input. Capture/Reload trigger for Counter 2 and also functions as an Up/Down control input for Counter 2.
SS	I	Slave Select Input for the SPI Interface
SDATA	I/O	User Selectable, I^2C-Compatible or SPI Data Input/Output Pin
SCLOCK	I/O	Serial Clock Pin for I^2C-Compatible or SPI Serial Interface Clock
MOSI	I/O	SPI Master Output/Slave Input Data I/O Pin for SPI Interface
MISO	I/O	SPI Master Input/Slave Output Data I/O Pin for SPI Serial Interface
DAC0	O	Voltage Output from DAC0
DAC1	O	Voltage Output from DAC1
RESET	I	Digital Input. A high level on this pin for 24 master clock cycles while the oscillator is running resets the device.
P3.0–P3.7	I/O	Port 3 is a bidirectional port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. Port 3 pins also contain various secondary functions which are described below.
PWMC	I	PWM Clock Input
PWM0	O	PMW0 Voltage Output. PWM outputs can be configured to use ports 2.6 & 2.7 or 3.4 and 3.3
PWM1	O	PMW1 Voltage Ouput. See CFG832 Register for further Information.
RxD	I/O	Receiver Data Input (Asynchronous) or Data Input/Output (Synchronous) of Serial (UART) Port
TxD	O	Transmitter Data Output (Asynchronous) or Clock Output (Synchronous) of Serial (UART) Port
INT0	I	Interrupt 0, programmable edge or level triggered Interrupt input, which can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 0.
INT1	I	Interrupt 1, programmable edge or level triggered Interrupt input, which can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 1.
T0	I	Timer/Counter 0 Input
T1	I	Timer/Counter 1 Input
CONVST	I	Active low Convert Start Logic input for the ADC block when the external Convert start function is enabled. A low-to-high transition on this input puts the track/hold into its hold mode and starts conversion.
WR	O	Write Control Signal, Logic Output. Latches the data byte from Port 0 into the external data memory.
RD	O	Read Control Signal, Logic Output. Enables the external data memory to Port 0.
XTAL2	O	Output of the Inverting Oscillator Amplifier
XTAL1	I	Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
DGND	G	Digital Ground. Ground reference point for the digital circuitry.
P2.0–P2.7 (A8–A15) (A16–A23)	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the external 24-bit external data memory space.

PIN FUNCTION DESCRIPTION (continued)

Mnemonic	Type	Function
PSEN	O	Program Store Enable, Logic Output. This output is a control signal that enables the external program memory to the bus during external fetch operations. It is active every six oscillator periods except during external data memory accesses. This pin remains high during internal program execution. PSEN can also be used to enable serial download mode when pulled low through a resistor on power-up or RESET.
ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit address space accesses) of the address into external memory during normal operation.
EA	I	External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to 1FFFH. When held low this input enables the device to fetch all instructions from external program memory. This pin should not be left float.
P0.7–P0.0	I/O	Port 0 is an 8-Bit Open Drain Bidirectional I/O port. Port 0 pins that have 1s written to them float and in that state can be used as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-ups when emitting 1s.

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity

This is the maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., +1/2 LSB.

Gain Error

This is the deviation of the last code transition from the ideal AIN voltage (Full Scale – 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise +distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total Harmonic Distortion is the ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

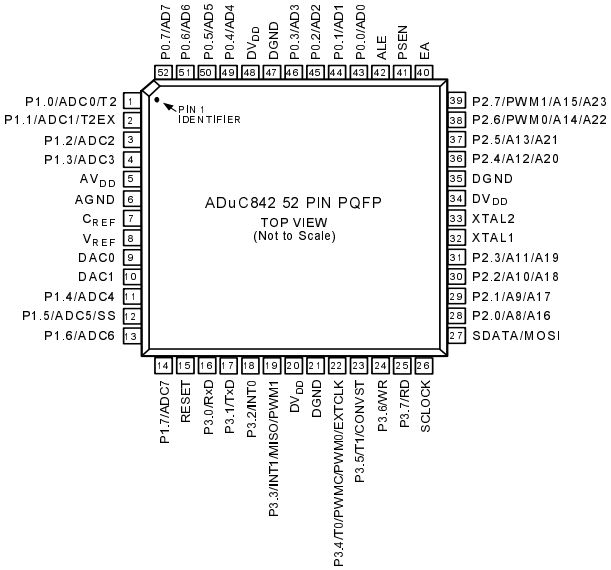
Voltage Output Settling Time

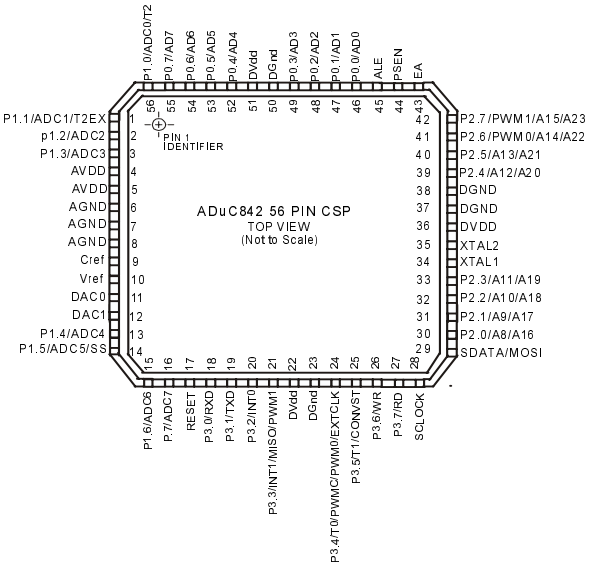
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV sec.

PIN CONFIGURATION





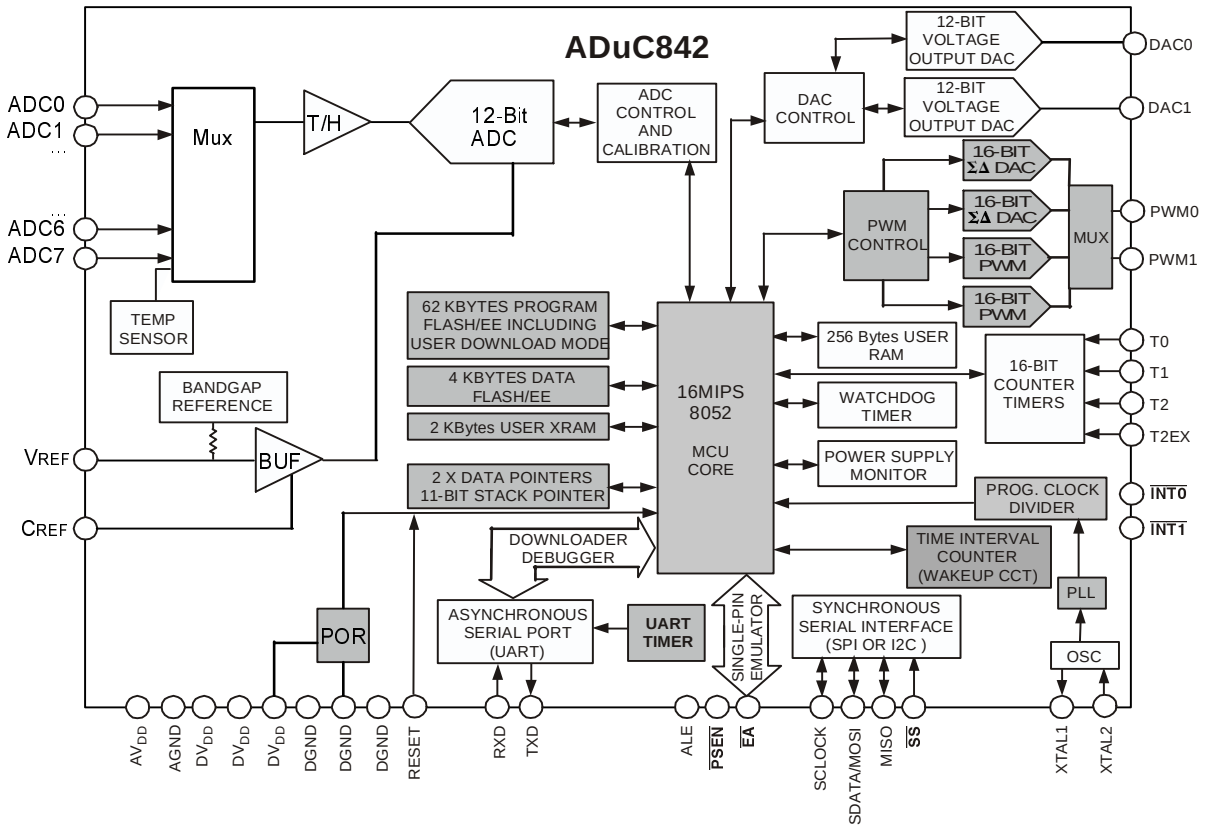


Figure 1 ADuC842 Block Diagram (Shaded areas are features not present on the ADuC812)

ADuC842

INTRODUCTION

The ADuC842 is a 16MIPs 8052 core upgrade to the ADuC832. It has all the same features as the ADuC832 but the standard 12-cycle 8052 core has been replaced with a 16MIPs single cycle core.

Since the ADuC842 and ADuC832 share the same feature set only the differneces bettween the two chips are documented here. For full documentation on the ADuC832 please consult the datasheet available at
http://www.analog.com/microconverter

8052 Instruction Set

The following pages document the number of clock cycles required for each instruction. Most instructions are executed in one or two clock cycles resulting in a 16MIPs peak peformance when operating at PLLCON = 00H.

Timer Operation

Timers on a standard 8052 increment by one with each machine cycle. On the ADuC842 one machine cycle is equal to one clock cycle hence the timers will increment at the same rate as the core clock.

ALE

The output on the ALE pin on the ADuC832 was a clock at 1/6th of the core operating frequency. On the ADuC842 the ALE pin operates as follows.

For a single machine cycle instruction: ALE is high for the first half of the machine cycle and low for the second half. The ALE output is at the core operating frequency.

For a two or more machine cycle instruction: ALE is high for the first half of the first machine cycle and then low for the rest of the machine cycles.

External Memory Access

There is no support for external program memory access on the ADuC842. When accessing external RAM the EWAIT register may need to be programmed in order to give extra machine cycles to MOVX commands. This is to account for differing external RAM access speeds.

Baud Rate Generation

There is an addition divide by two in the fractional divider of the ADuC842 this means that any values calculated for T3CON for the ADuC832 need to be incremented by one in order to give the same baud rate on the ADuC842.

INSTRUCTION TABLE

Mnemonic	Description	Bytes	Cycles
Arithmetic			
ADD A,Rn	Add register to A	1	1
ADD A,@Ri	Add indirect memory to A	1	2
ADD A,dir	Add direct byte to A	2	2
ADD A,#data	Add immediate to A	2	2
ADDC A,Rn	Add register to A with carry	1	1
ADDC A,@Ri	Add indirect memory to A with carry	1	2
ADDC A,dir	Add direct byte to A with carray	2	2
ADD A,#data	Add immediate to A with carry	2	2
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2
SUBB A,dir	Subtract direct from A with borrow	2	2
SUBB A,#data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC @Ri	Increment indirect memory	1	2
INC dir	Increment direct byte	2	2
INC DPTR	Increment data pointer	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement Register	1	1
DEC @Ri	Decrement indirect memory	1	2
DEC dir	Decrement direct byte	2	2
MUL AB	Multiply A by B	1	9
DIV AB	Divide A by B	1	9
DA A	Decimal Adjust A	1	2
Logic			
ANL A,Rn	AND register to A	1	1
ANL A,@Ri	AND indirect memory to A	1	2
ANL A,dir	AND direct byte to A	2	2
ANL A,#data	AND immediate to A	2	2
ANL dir,A	AND A to direct byte	2	2
ANL dir,#data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to A	1	1
ORL A,@Ri	OR indirect memory to A	1	2
ORL A,dir	OR direct byte to A	2	2
ORL A,#data	OR immediate to A	2	2
ORL dir,A	OR A to direct byte	2	2
ORL dir,#data	OR immediate data to direct byte	3	3

XRL A,Rn	Exclusive-OR register to A	1	1
XRL A,@Ri	Exclusive-OR indirect memory to A	2	2
XRL A,#data	Exclusive-OR immediate to A	2	2
XRL dir,A	Exclusive-OR A to direct byte	2	2
XRL A,dir	Exclusive-OR indirect memory to A	2	2
XRL dir,#data	Exclusive-OR immediate data to direct	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
SWAP A	Swap Nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer			
MOV A,Rn	Move register to A	1	1
MOV A,@Ri	Move indirect memory to A	1	2
MOV Rn,A	Move A to register	1	1
MOV @Ri,A	Move A to indirect memory	1	2
MOV A,dir	Move direct byte to A	2	2
MOV A,#data	Move immediate to A	2	2
MOV Rn,#data	Move register to immediate	2	2
MOV dir,A	Move A to direct byte	2	2
MOV Rn, dir	Mov register to direct byte	2	2
MOV dir, Rn	Move direct to register	2	2
MOV @Ri,#data	Move immediate to indirect memory	2	2
MOV dir,dir	Move direct byte to direct byte	3	3
MOV dir,#data	Move immediate to direct byte	3	3
MOV DPTR,#data	Move immediate to data pointer	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A,@A+PC	Move code byte relative PC to A	1	4
MOVX A,@Ri	Move external (A8) data to A	1	4
MOVX A,@DPTR	Move external (A16) data to A	1	4
MOVX @Ri,A	Move A to external data (A8)	1	4
MOVX @DPTR,A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A,Rn	Exchange A and register	1	1
XCH A,@Ri	Exchange A and indirect memory	1	2
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2
XCH A,dir	Exchange A and direct byte	2	2
Boolean			

CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit and carry	2	2
ANL C,/bit	AND direct bit inverse to carry	2	2
ORL C,bit	OR direct bit and carry	2	2
ORL C,/bit	OR direct bit inverse to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry = 1	2	3
JNC rel	Jump on carry = 0	2	3
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator != 0	2	3
DJNZ Rn,rel	Decrement register, jnz relative	2	3
LJMP	Long jump unconditional	3	4
LCALL addr16	Long jump to subroutine	3	4
JB bit,rel	Jump on direct bit = 1	3	4
JNB bit,rel	Jump on direct bit = 0	3	4
JBC bit,rel	Jump on direct bit = 1 and clear	3	4
CJNE A,dir,rel	Compare A, direct JNE relative	3	4
CJNE A,#data,rel	Compare A, immediate JNE relative	3	4
CJNE Rn,#data,rel	Compare register, immediate JNE relative	3	4
CJNE @Ri,#data,rel	Compare indirect, immediate JNE relative	3	4
DJNZ dir,rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous			
NOP	No operation	1	1

Notes:

1. One cycle is one clock.

2. Cycles of MOVX instructions are 4 cycles when they have 0 wait state. Cycles of MOVX instructions are 4+n cycles when they have n wait states.

3. Cycles of LCALL instruction are 3 cycles when the LCALL instruction comes from interrupt.

ADuC842

I²C-COMPATIBLE INTERFACE

The ADuC842 supports a fully licensed* I²C serial interface. The I²C interface is implemented as a full hardware slave and software master. SDATA is the data I/O pin and SCLOCK is the serial clock. These two pins are shared with the MOSI and SCLOCK pins of the on-chip SPI interface.

To enable the I2C interface the SPI interface must be turned off (see SPE in SPICON previously) OR the SPI interface must be moved to P3.3, P3.4 and P3.5 via the CFG841.1 bit. Application Note uC001 describes the operation of this interface as implemented is available from the MicroConverter Website at www.analog.com/microconverter.

Three SFRs are used to control the I²C interface. These are described below:

I2CCON:	**I²C Control Register**
SFR Address	E8H
Power-On Default Value	00H
Bit Addressable	Yes

Table I2CCON SFR Bit Designations Master Mode

Bit		Name	Description
7	MDO		I²C Software Master Data Output Bit (MASTER MODE ONLY). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit will be outputted on the SDATA pin if the data output enable (MDE) bit is set.
6	MDE		I²C Software Master Data Output Enable Bit (MASTER MODE ONLY). *Set* by user to enable the SDATA pin as an output (Tx). *Cleared* by the user to enable SDATA pin as an input (Rx).
5	MCO		I²C Software Master Clock Output Bit (MASTER MODE ONLY). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit will be outputted on the SCLOCK pin.
4	MDI		I²C Software Master Data Input Bit (MASTER MODE ONLY). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on SCLOCK if the Data Output Enable (MDE) bit is '0.'
3	I2CM		I²C Master/Slave Mode Bit. *Set* by user to enable I²C software master mode. *Cleared* by user to enable I²C hardware slave mode.
2	----		RSVD
1	----		RSVD
0	----		RSVD

Table I2CCON SFR Bit Designations Slave Mode

Bit		Name	Description
7	I2CSI		I²C Stop Interrupt Enable Bit. Set by the user to enable I2C stop interrupts. If set a stop bit that follows a valid start condition will generate an interrupt. Cleared by the user to disable I2C stop interrupts.
6	I2CGC		I²C General Call Status Bit *Set* by hardware after receiving a general call address. *Cleared* by the user.
5	I2CID1		I²C Interrupt Decode Bits.
4	I2CID0		Set by hardware to indicate the source of an I2C interrupt 00 Start and Matching Address 01 Repeated Start and Matching Address 10 User Data 11 Stop after a Start and Matching Address
3	I2CM		I²C Master/Slave Mode Bit. *Set* by user to enable I²C software master mode. *Cleared* by user to enable I²C hardware slave mode.
2	I2CRS		I²C Reset Bit (SLAVE MODE ONLY). *Set* by user to reset the I²C interface. *Cleared* by user code for normal I²C operation.
1	I2CTX		I²C Direction Transfer Bit (SLAVE MODE ONLY). *Set* by the MicroConverter if the interface is transmitting.

		Cleared by the MicroConverter if the interface is receiving.
0	I2CI	I^2C Interrupt Bit (SLAVE MODE ONLY). *Set* by the MicroConverter after a byte has been transmitted or received. *Cleared* automatically when user code reads the I2CDAT SFR (see I2CDAT below).

I2CADD — **I^2C Address Register**

Function: Holds the first I^2C peripheral address for the part. It may be overwritten by user code. Technical NoteuC001 at www.analog.com/microconverter describes the format of the I^2C standard 7-bit address in detail.

SFR Address: 9BH
Power-On Default Value: 55H
Bit Addressable: No

I2CADD1 — **I^2C Address Register**

Function: Holds the second I^2C peripheral address for the part. It may be overwritten by user code.

SFR Address: 91H
Power-On Default Value: 00H
Bit Addressable: No

I2CADD2 — **I^2C Address Register**

Function: Holds the third I^2C peripheral address for the part. It may be overwritten by user code.

SFR Address: 92H
Power-On Default Value: 00H
Bit Addressable: No

I2CADD3 — **I^2C Address Register**

Function: Holds the fourth I^2C peripheral address for the part. It may be overwritten by user code.

SFR Address: 93H
Power-On Default Value: 00H
Bit Addressable: No

I2CDAT — **I^2C Data Register**

Function: The I2CDAT SFR is written by the user to transmit data over the I^2C interface or read by user code to read data just received by the I^2C interface. Accessing I2CDAT automatically clears any pending I^2C interrupt and the I2CI bit in the I2CCON SFR. User software should only access I2CDAT once perinterrupt cycle.

SFR Address: 9AH
Power-On Default Value: 00H
Bit Addressable: No

* Purchase of licensed I^2C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I^2C

Patent Rights to use the ADuC842 in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

ADuC842

The main features of the MicroConverter I²C interface are:

- Only two bus lines are required; a serial data line (SDATA) and a serial clock line (SCLOCK).
- An I²C master can communicate with multiple slave devices. Because each slave device has a unique 7-bit address then single master/slave relationships can exist at all times even in a multi slave environment
- Ability to respond to 4 seperate addresses when operating in slave mode
- An I²C slave can respond to repeated start conditions without a stop bit in between. This allows a master to change direction of transfer without giving up the bus.
- On-Chip filtering rejects <50ns spikes on the SDATA and the SCLOCK lines to preserve data integrity.

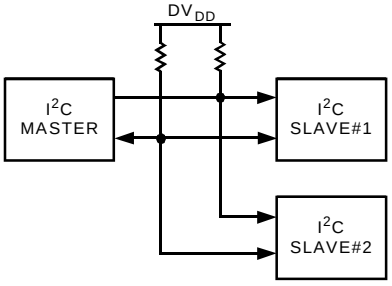


Figure 36. Typical I²C System

Software Master Mode

The ADuC841 can be used as a I²C master device by configuring the I²C peripheral in master mode and writing sotware to output the data bit by bit. This is referred to as a software master. Master mode is enabled by setting the I2CM bit in the I2CCON register.

To transmit data on the SDATA line, MDE must be set to enable the output driver on the SDATA pin. If MDE is set then the SDATA pin will be pulled high or low depending on whether the MDO bit is set or cleared. MCO controls the SCLOCK pin and is always configured as an output in master mode. In master mode the SCLOCK pin will be pulled high or low depending on the whether MCO is set or cleared.

To receive data, MDE must be cleared to disable the output driver on SDATA. Software must provide the clocks by toggling the MCO bit and read SDATA pin via the MDI bit. If MDE is cleared MDI can be used to read the SDATA pin. The value of the SDATA pin is latched into MDI on a rising edge pf SCLOCK. MDI is set if the SDATA pin was high on the last rising edge of SCLOCK. MDI is clear if the SDATA pin was low on the last rising edge of SCLOCK.

Software must control MDO, MCO and MDE appropriately to generate the START condition, slave address, acknowledge bits, data bytes and STOP conditions appropriately. These functions are provided in tech note uC001.

Hardware Slave Mode

After reset the ADuC842 defaults to hardware slave mode. The I²C interface is enabled by clearing the SPE bit in SPICON. Slave mode is enabled by clearing the I2CM bit in I2CCON. The ADuC842 has a full hardware slave. In slave mode the I²C address is stored in the I2CADD register. Data received or to be transmitted is stored in the I2CDAT register.

Once enabled in I²C slave mode the slave controller waits for a START condition. If the ADuC842 detects a valid start condition, followed by a valid address, followed by the R/$\overline{W}$ bit the I2CI interrupt bit will get automatically set by hardware.

The I²C peripheral will only generate a core interrupt if the user has pre-configured the I²C interrupt enable bit in the IEIP2 SFR as well as the global interrupt bit EA in the IE SFR. i.e.

```
; Enabling I2C Interrupts for the ADuC831
MOV   IEIP2,#01h       ; enable I2C interrupt
SETB  EA
```

On the ADuC841 an auto-clear of the I2CI bit is implemented so this bit is cleared automatically on a read or write access to the I2CDAT SFR.

```
MOV        I2CDAT, A     ; I2CI auto-cleared
MOV        A, I2CDAT     ; I2CI auto-cleared
```

If for any reason the user tries to clear the interrupt more than once i.e. access the data SFR more than once per interrupt then the I²C controller will halt. The interface will then have to be reset using the I2CRS bit.

The user can choose to poll the I2CI bit or enable the interrupt. In the case of the interrupt the PC counter will vector to 003BH at the end of each complete byte. For the first byte when the user gets to the I2CI ISR the 7-bit address and the R/$\overline{W}$ bit will appear in the I2CDAT SFR.

The I2CTX bit contains the R/$\overline{W}$ bit sent from the master. If I2CTX is set then the master would like to receive a byte. Hence the slave will transmit data by writing to the I2CDAT register. If I2CTX is cleared the master would like to transmit a byte. Hence the slave will receive a serial byte. Software can interrogate the state of I2CTX to determine whether is should write to or read from I2CDAT.

Once the ADuC842 has received a valid address, hardware will hold SCLOCK low until the I2CI bit is cleared by software. This allows the master to wait for the slave to be ready before transmitting the clocks for the next byte.

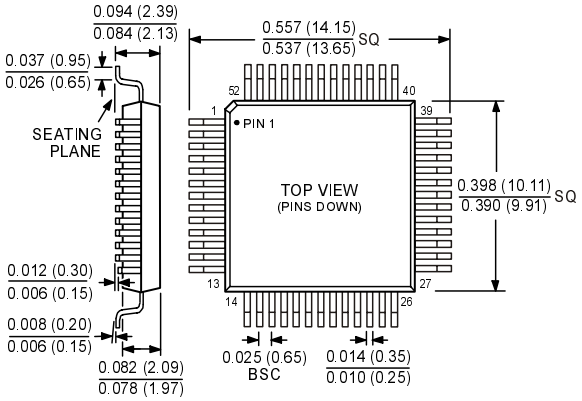
The I2CI interrupt bit will be set every time a complete data byte is received or transmitted provided it is followed by a valid ACK. If the byte is followed by a NACK an interrupt is NOT generated. The ADuC842 will continue to issue interrupts for each complete data byte transferred until a STOP condition is received or the interface is reset.

When a STOP condition is received, the interface will reset to a state where it is waiting to be addressed (idle). Similarly, if the interface receives a NACK at the end of a sequence it also returns to the default idle state. The I2CRS bit can be used to reset the I²C interface. This bit can be used to force the interface back to the default idle state.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

52-Lead Plastic Quad Flatpack
(S-52)



56Lead Chip Scale Package(CP-56)